Application No.: 10/779,781

Reply dated July 2, 2007

Response to Ex parte Quayle Action of June 4, 2007

AMENDMENTS TO THE CLAIMS

Please **CANCEL** claims 5, 6, 9-12, and 14-47 without prejudice or disclaimer.

Please **AMEND** claim 2 as shown below.

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Canceled)

2. (Currently Amended) The flat panel display device with polycrystalline silicon thin film

transistor according to claim [[1]] 4, wherein a shape of the grains of polycrystalline silicon is

anisotropic, and the grain boundaries are primary grain boundaries.

3. (Previously Presented) The flat panel display device with polycrystalline silicon thin

film transistors according to claim 4, wherein a shape of the grains of polycrystalline silicon is

anisotropic, and the grain boundaries include side grain boundaries of anisotropic grains.

4. (Previously Presented) A flat panel display device with polycrystalline silicon thin film

transistors, comprising:

a pixel portion divided by gate lines and data lines and comprising thin film transistors

driven by signals applied by the gate lines and data lines; and

a driving circuit portion comprising thin film transistors connected to the gate lines and

data lines respectively to apply signals to the pixel portion,

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wherein an average number of grain boundaries of polycrystalline silicon formed in an

active channel region of each thin film transistor installed at the driving circuit portion and meet

a current direction line is at least one or more less than an average number of grain boundaries

of polycrystalline silicon formed in an active channel region of each thin film transistor installed

at the pixel portion and meet a current direction line for a unit area of active channels,

wherein the polycrystalline silicon grain boundaries formed in the active channel region

of each thin film transistor installed at the driving circuit portion include primary polycrystalline

silicon grain boundaries that are inclined to the current direction line at an angle of about – 45 to

45°,

wherein the polycrystalline silicon grain boundaries formed in the active channel region

of each thin film transistor installed at the pixel portion include primary polycrystalline silicon

grain boundaries that are inclined to the current direction line at an angle of about – 45 to 45°,

and

wherein the active channel of each thin film transistor installed at the pixel portion is

longer than the active channel of each thin film transistor installed at the driving circuit portion.

5-6. (Canceled)

7. (Previously Presented) The flat panel display device with polycrystalline silicon thin

film transistor according to claim 2, wherein the polycrystalline silicon is fabricated by a

sequential lateral solidification method.

8. (Previously Presented) The flat panel display device with polycrystalline silicon thin

film transistors according to claim 3, wherein the polycrystalline silicon is fabricated by a metal

induced lateral crystallization method.

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9-12. (Canceled)

13. (Previously Presented) The flat panel display device with polycrystalline silicon thin film transistors according to claim 4, wherein the flat panel display device is one of an organic electroluminescent device and a liquid crystal display device.

14-48. (Canceled)